MSP432P4xx pin attributes descriptions

SIGNAL NAME	PIN (PZ)	Arduino	GPIO	ADC	Timer	UART	I2C	SPI	Clock	Port Mapper	Comparator	LCD
P1.0/UCA0STE/L19	4	78	P1.0					UCA0STE				L19
P1.1/UCA0CLK/L18	5	73	P1.1					UCA0CLK				L18
P1.2/UCA0RXD/UCA0SOMI/L17	6	RXD	P1.2			UCA0RXD		UCA0SOMI				L17
P1.3/UCA0TXD/UCA0SIMO/L16	7	TXD	P1.3			UCA0TXD		UCA0SIMO				L16
P1.4/UCB0STE/L15	8	74	P1.4					UCB0STE				L15
P1.5/UCB0CLK/L14	9	7	P1.5					UCB0CLK				L14
P1.6/UCB0SDA/UCB0SIMO/L13	10	15	P1.6				UCB0SDA	UCB0SIMO				L13
P1.7/UCB0SCL/UCB0SOMI/L12	11	14	P1.7				UCB0SCL	UCB0SOMI				L12
P2.0/PM_UCA1STE/L11	16	75	P2.0							PM_UCA1STE		L11
P2.1/PM_UCA1CLK/L10	17	76	P2.1							PM_UCA1CLK		L10
P2.2/PM_UCA1RXD/PM_UCA1SOMI/L9	18	77	P2.2							PM_UCA1RXD/PM_UCA1SOMI		L9

SIGNAL NAME	Debug	Power	RTC	Reference	System	DESCRIPTION
P1.0/UCA0STE/L19						LCD drive pin 19 for either segment or common output General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability Slave transmit enable for eUSCI_A0 SPI mode
P1.1/UCA0CLK/L18						LCD drive pin 18 for either segment or common output General-purpose digital I/O with port interrupt and wake-up capability Clock signal input for eUSCI_A0 SPI slave mode. Clock signal output for eUSCI_A0 SPI master mode
P1.2/UCA0RXD/UCA0SOMI/L17						LCD drive pin 17 for either segment or common output General-purpose digital I/O with port interrupt and wake-up capability Slave out, master in for eUSCI_A0 SPI mode Receive data for eUSCI_A0 UART mode
P1.3/UCA0TXD/UCA0SIMO/L16						LCD drive pin 16 for either segment or common output General-purpose digital I/O with port interrupt and wake-up capability Slave in, master out for eUSCI_A0 SPI mode Transmit data for eUSCI_A0 UART mode
P1.4/UCB0STE/L15						LCD drive pin 15 for either segment or common output General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability Slave transmit enable for eUSCI_B0 SPI mode
P1.5/UCB0CLK/L14						LCD drive pin 14 for either segment or common output General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability Clock signal input for eUSCI_B0 SPI slave mode. Clock signal output for eUSCI_B0 SPI master mode
P1.6/UCB0SDA/UCB0SIMO/L13						LCD drive pin 13 for either segment or common output General-purpose digital I/O with port interrupt and wake-up capability I2C data in eUSCI_B0 I2C mode Slave in, master out for eUSCI_B0 SPI mode
P1.7/UCB0SCL/UCB0SOMI/L12						LCD drive pin 12 for either segment or common output General-purpose digital I/O with port interrupt and wake-up capability I2C clock in eUSCI_B0 I2C mode Slave out, master in for eUSCI_B0 SPI mode
P2.0/PM_UCA1STE/L11						LCD drive pin 11 for either segment or common output General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function. This I/O can be configured for high drive operation with a drive capability of up to 20 mA. Default mapping: Slave transmit enable for eUSCI_A1 SPI mode
P2.1/PM_UCA1CLK/L10						LCD drive pin 10 for either segment or common output General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function. This I/O can be configured for high drive operation with a drive capability of up to 20 mA. Default mapping: Clock signal input in eUSCI_A1 SPI slave mode. Clock signal output in eUSCI_A1 SPI master mode
P2.2/PM_UCA1RXD/PM_UCA1SOMI/L9						LCD drive pin 9 for either segment or common output General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function. This I/O can be configured for high drive operation with a drive capability of up to 20 mA. Default mapping: Receive data in eUSCI_A1 UART mode Default mapping: Slave out, master in for eUSCI_A1 SPI mode

MSP432P4xx pin attributes descriptions

SIGNAL NAME	PIN (PZ)	Arduino	GPIO	ADC	Timer	UART	I2C	SPI	Clock	Port Mapper	Comparator	LCD
P2.3/PM_UCA1SIMO/PM_UCA1TXD/L8	19	34	P2.3							PM_UCA1SIMO/PM_UCA1TXD		L8
P2.4/PM_TA0.1/L23	20	38	P2.4							PM_TA0.1		L23
P2.5/PM_TA0.2/L22	21	19	P2.5							PM_TA0.2		L22
P2.6/PM_TA0.3/L21	22	39	P2.6							PM_TA0.3		L21
P2.7/PM_TA0.4/L20	23	40	P2.7							PM_TA0.4		L20
P3.0/PM_UCA2STE/L7	32	18	P3.0							PM_UCA2STE		L7
P3.1/PM_UCA2CLK/L6	33		P3.1							PM_UCA2CLK		L6
P3.2/PM_UCA2RXD/PM_UCA2SOMI/L5	34	3	P3.2							PM_UCA2RXD/PM_UCA2SOMI		L5
P3.3/PM_UCA2SIMO/PM_UCA2TXD/L4	35	4	P3.3							PM_UCA2SIMO/PM_UCA2TXD		L4
P3.4/PM_UCB2STE/L3	36		P3.4							PM_UCB2STE		L3

SIGNAL NAME	Debug	Power	RTC	Reference	System	DESCRIPTION
P2.3/PM_UCA1SIMO/PM_UCA1TXD/L8						LCD drive pin 8 for either segment or common output General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function. This I/O can be configured for high drive operation with a drive capability of up to 20 mA. Default mapping: Slave in, master out for eUSCI_A1 SPI mode Default mapping: Transmit data for eUSCI_A1 UART mode
P2.4/PM_TA0.1/L23						LCD drive pin 23 for either segment or common output General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function Default mapping: TA0 CCR1 capture: CCI1A input, compare: Out1
P2.5/PM_TA0.2/L22						LCD drive pin 22 for either segment or common output General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function Default mapping: TA0 CCR2 capture: CCI2A input, compare: Out2
P2.6/PM_TA0.3/L21						LCD drive pin 21 for either segment or common output General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function Default mapping: TA0 CCR3 capture: CCI3A input, compare: Out3
P2.7/PM_TA0.4/L20						LCD drive pin 20 for either segment or common output General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function Default mapping: TA0 CCR4 capture: CCI4A input, compare: Out4
P3.0/PM_UCA2STE/L7						LCD drive pin 7 for either segment or common output General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability, and with reconfigurable port mapping secondary function Default mapping: Slave transmit enable for eUSCI_A2 SPI mode
P3.1/PM_UCA2CLK/L6						LCD drive pin 6 for either segment or common output General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function Default mapping: Clock signal input for eUSCI_A2 SPI slave mode. Clock signal output for eUSCI_A2 SPI master mode
P3.2/PM_UCA2RXD/PM_UCA2SOMI/L5						LCD drive pin 5 for either segment or common output General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function Default mapping: Receive data for eUSCI_A2 UART mode Default mapping: Slave out, master in for eUSCI_A2 SPI mode
P3.3/PM_UCA2SIMO/PM_UCA2TXD/L4						LCD drive pin 4 for either segment or common output General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function Default mapping: Slave in, master out for eUSCI_A2 SPI mode Default mapping: Transmit data for eUSCI_A2 UART mode
P3.4/PM_UCB2STE/L3						LCD drive pin 3 for either segment or common output General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability, and with reconfigurable port mapping secondary function Default mapping: Slave transmit enable for eUSCI_B2 SPI mode

MSP432P4xx pin attributes descriptions

SIGNAL NAME	PIN (PZ)	Arduino	GPIO	ADC	Timer	UART	I2C	SPI	Clock	Port Mapper	Comparator	LCD
P3.5/PM_UCB2CLK/L2	37	32	P3.5							PM_UCB2CLK		L2
P3.6/PM_UCB2SDA/PM_UCB2SIMO/L1	38	11	P3.6							PM_UCB2SDA/PM_UCB2SIMO		L1
P3.7/PM_UCB2SCL/PM_UCB2SOMI/L0	39	31	P3.7							PM_UCB2SCL/PM_UCB2SOMI		L0
P4.0/A13/L13	56	24	P4.0	A13								L13
P4.1/A12/L12	57	5	P4.1	A12								L12
P4.2/A11/TA2CLK/ACLK	58	25	P4.2	A11	TA2CLK				ACLK			
P4.3/A10/MCLK/RTCCLK	59	6	P4.3	A10					MCLK			
P4.4/A9/HSMCLK/SVMHOUT	60	26	P4.4	A9					HSMCLK			
P4.5/A8	61	27	P4.5	A8								
P4.6/A7	62	8	P4.6	A7								
P4.7/A6	63	28	P4.7	A6								
P5.0/A5	64	13	P5.0	A5								
P5.1/A4	65	33	P5.1	A4								
P5.2/A3	66	12	P5.2	A3								
P5.3/A2	67	61	P5.3	A2								
P5.4/A1	68	29	P5.4	A1								

SIGNAL NAME	Debug	Power	RTC	Reference	System	DESCRIPTION
P3.5/PM_UCB2CLK/L2						LCD drive pin 2 for either segment or common output General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability, and with reconfigurable port mapping secondary function Default mapping: Clock signal input for eUSCI_B2 SPI slave mode. Clock signal output for eUSCI_B2 SPI master mode
P3.6/PM_UCB2SDA/PM_UCB2SIMO/L1						LCD drive pin 1 for either segment or common output General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function Default mapping: I2C data for eUSCI_B2 I2C mode Default mapping: Slave in, master out for eUSCI_B2 SPI mode
P3.7/PM_UCB2SCL/PM_UCB2SOMI/L0						LCD drive pin 0 for either segment or common output General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function Default mapping: I2C clock for eUSCI_B2 I2C mode Default mapping: Slave out, master in for eUSCI_B2 SPI mode
P4.0/A13/L13						ADC analog input A13 General-purpose digital I/O with port interrupt and wake-up capability
P4.1/A12/L12						ADC analog input A12 General-purpose digital I/O with port interrupt and wake-up capability
P4.2/A11/TA2CLK/ACLK						ADC analog input A11 ACLK clock output General-purpose digital I/O with port interrupt and wake-up capability TA2 input clock
P4.3/A10/MCLK/RTCCLK			RTCCLK			ADC analog input A10 MCLK clock output General-purpose digital I/O with port interrupt and wake-up capability RTC_C clock calibration output
P4.4/A9/HSMCLK/SVMHOUT					SVMHOUT	ADC analog input A9 HSMCLK clock output General-purpose digital I/O with port interrupt and wake-up capability SVMH output
P4.5/A8						ADC analog input A8 General-purpose digital I/O with port interrupt and wake-up capability
P4.6/A7						ADC analog input A7 General-purpose digital I/O with port interrupt and wake-up capability
P4.7/A6						ADC analog input A6 General-purpose digital I/O with port interrupt and wake-up capability
P5.0/A5						ADC analog input A5 General-purpose digital I/O with port interrupt and wake-up capability
P5.1/A4						ADC analog input A4 General-purpose digital I/O with port interrupt and wake-up capability
P5.2/A3						ADC analog input A3 General-purpose digital I/O with port interrupt and wake-up capability
P5.3/A2						ADC analog input A2 General-purpose digital I/O with port interrupt and wake-up capability
P5.4/A1						ADC analog input A1 General-purpose digital I/O with port interrupt and wake-up capability

MSP432P4xx pin attributes descriptions

SIGNAL NAME	PIN (PZ)	Arduino	GPIO	ADC	Timer	UART	I2C	SPI	Clock	Port Mapper	Comparator	LCD
P5.5/A0	69	30	P5.5	A0								
P5.6/TA2.1/C1.7/VREF+	70	37	P5.6		TA2.1						C1.7	
P5.7/TA2.2/C1.6/VREF-	71	17	P5.7		TA2.2						C1.6	
P6.0/A15/L15	54	2	P6.0	A15								L15
P6.1/A14/L14	55	23	P6.1	A14								L14
P6.2/UCB1STE/C1.5/L27	76	46	P6.2					UCB1STE			C1.5	L27
P6.3/UCB1CLK/C1.4/L26	77	63	P6.3					UCB1CLK			C1.4	L26
P6.4/UCB1SDA/UCB1SIMO/C1.3/L25	78	10	P6.4				UCB1SDA	UCB1SIMO			C1.3	L25
P6.5/UCB1SCL/UCB1SOMI/C1.2/L24	79	9	P6.5				UCB1SCL	UCB1SOMI			C1.2	L24
P6.6/TA2.3/UCB3SDA/UCB3SIMO/C1.1	80	36	P6.6		TA2.3		UCB3SDA	UCB3SIMO			C1.1	
P6.7/TA2.4/UCB3SCL/UCB3SOMI/C1.0	81	35	P6.7		TA2.4		UCB3SCL	UCB3SOMI			C1.0	

SIGNAL NAME	Debug	Power	RTC	Reference	System	DESCRIPTION
P5.5/A0						ADC analog input A0 General-purpose digital I/O with port interrupt and wake-up capability
P5.6/TA2.1/C1.7/VREF+				VREF+		Comparator_E1 input 7 General-purpose digital I/O with port interrupt and wake-up capability Internal shared reference voltage positive terminal Positive terminal of external reference voltage to ADC TA2 CCR1 capture: CCI1A input, compare: Out1
P5.7/TA2.2/C1.6/VREF-				VREF-		Comparator_E1 input 6 General-purpose digital I/O with port interrupt and wake-up capability Internal shared reference voltage negative terminal Negative terminal of external reference voltage to ADC (recommended to connect to onboard ground) TA2 CCR2 capture: CCI2A input, compare: Out2
P6.0/A15/L15						ADC analog input A15 General-purpose digital I/O with port interrupt and wake-up capability
P6.1/A14/L14						ADC analog input A14 General-purpose digital I/O with port interrupt and wake-up capability
P6.2/UCB1STE/C1.5/L27						Comparator_E1 input 5 LCD drive pin 27 for either segment or common output General-purpose digital I/O with port interrupt and wake-up capability Slave transmit enable for eUSCI_B1 SPI mode
P6.3/UCB1CLK/C1.4/L26						Comparator_E1 input 4 LCD drive pin 26 for either segment or common output General-purpose digital I/O with port interrupt and wake-up capability Clock signal input for eUSCI_B1 SPI slave mode. Clock signal output for eUSCI_B1 SPI master mode
P6.4/UCB1SDA/UCB1SIMO/C1.3/L25						Comparator_E1 input 3 LCD drive pin 25 for either segment or common output General-purpose digital I/O with port interrupt and wake-up capability I2C data in eUSCI_B1 I2C mode Slave in, master out for eUSCI_B1 SPI mode
P6.5/UCB1SCL/UCB1SOMI/C1.2/L24						Comparator_E1 input 2 LCD drive pin 24 for either segment or common output General-purpose digital I/O with port interrupt and wake-up capability I2C clock in eUSCI_B1 I2C mode Slave out, master in for eUSCI_B1 SPI mode
P6.6/TA2.3/UCB3SDA/UCB3SIMO/C1.1						Comparator_E1 input 1 General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability I2C data in eUSCI_B3 I2C mode TA2 CCR3 capture: CCI3A input, compare: Out3
P6.7/TA2.4/UCB3SCL/UCB3SOMI/C1.0						Comparator_E1 input 0 General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability I2C clock in eUSCI_B3 I2C mode TA2 CCR4 capture: CCI4A input, compare: Out4

MSP432P4xx pin attributes descriptions

SIGNAL NAME	PIN (PZ)	Arduino	GPIO	ADC	Timer	UART	I2C	SPI	Clock	Port Mapper	Comparator	LCD
P7.0/PM_DMAE0/PM_SMCLK/R03	88	65	P7.0							PM_DMAE0/PM_SMCLK		R03
P7.1/PM_C0OUT/PM_TA0CLK/R13	89	48	P7.1							PM_C0OUT/PM_TA0CLK		R13
P7.2/PM_C1OUT/PM_TA1CLK/R23	90	64	P7.2							PM_C1OUT/PM_TA1CLK		R23
P7.3/PM_TA0.0	91	47	P7.3							PM_TA0.0		
P7.4/PM_TA1.4/C0.5/L31	26	52	P7.4							PM_TA1.4	C0.5	L31
P7.5/PM_TA1.3/C0.4/L30	27	68	P7.5							PM_TA1.3	C0.4	L30
P7.6/PM_TA1.2/C0.3/L29	28	53	P7.6							PM_TA1.2	C0.3	L29
P7.7/PM_TA1.1/C0.2/L28	29	69	P7.7		PM_TA1.1						C0.2	L28
P8.0/TA1.0/UCB3STE/C0.1	30	51	P8.0		TA1.0			UCB3STE			C0.1	
P8.1/TA2.0/UCB3CLK/C0.0	31		P8.1		TA2.0			UCB3CLK			C0.0	
P8.2/A23/TA3.2/L47	46	44	P8.2	A23	TA3.2							L47
P8.3/A22/TA3CLK/L46	47	60	P8.3	A22	TA3CLK							L46

SIGNAL NAME	Debug	Power	RTC	Reference	System	DESCRIPTION
P7.0/PM_DMAE0/PM_SMCLK/R03						Input port of fourth most positive analog LCD voltage V4 in external bias mode General-purpose digital I/O with reconfigurable port mapping secondary function (RD) Default mapping: DMA external trigger input Default mapping: SMCLK clock output
P7.1/PM_C0OUT/PM_TA0CLK/R13						Input port of fourth most positive analog LCD voltage V3 in external bias mode General-purpose digital I/O with reconfigurable port mapping secondary function (RD) Default mapping: Comparator_E0 output Default mapping: TA0 input clock
P7.2/PM_C1OUT/PM_TA1CLK/R23						Input port of fourth most positive analog LCD voltage V2 in external bias mode General-purpose digital I/O with reconfigurable port mapping secondary function (RD) Default mapping: Comparator_E1 output Default mapping: TA1 input clock
P7.3/PM_TA0.0						General-purpose digital I/O with reconfigurable port mapping secondary function (RD) Default mapping: TA0 CCR0 capture: CCI0A input, compare: Out0
P7.4/PM_TA1.4/C0.5/L31						Comparator_E0 input 5 LCD drive pin 31 for either segment or common output General-purpose digital I/O with reconfigurable port mapping secondary function (RD) Default mapping: TA1 CCR4 capture: CCI4A input, compare: Out4
P7.5/PM_TA1.3/C0.4/L30						Comparator_E0 input 4 LCD drive pin 30 for either segment or common output General-purpose digital I/O with reconfigurable port mapping secondary function (RD) Default mapping: TA1 CCR3 capture: CCI3A input, compare: Out3
P7.6/PM_TA1.2/C0.3/L29						Comparator_E0 input 3 LCD drive pin 29 for either segment or common output General-purpose digital I/O with reconfigurable port mapping secondary function (RD) Default mapping: TA1 CCR2 capture: CCI2A input, compare: Out2
P7.7/PM_TA1.1/C0.2/L28						Comparator_E0 input 2 LCD drive pin 28 for either segment or common output General-purpose digital I/O with reconfigurable port mapping secondary function (RD) Default mapping: TA1 CCR1 capture: CCI1A input, compare: Out1
P8.0/TA1.0/UCB3STE/C0.1						Comparator_E0 input 1 General-purpose digital I/O Slave transmit enable for eUSCI_B3 SPI mode TA1 CCR0 capture: CCI0A input, compare: Out0
P8.1/TA2.0/UCB3CLK/C0.0						Comparator_E0 input 0 General-purpose digital I/O TA2 CCR0 capture: CCI0A input, compare: Out0
P8.2/A23/TA3.2/L47						ADC analog input A23 LCD drive pin 47 for either segment or common output General-purpose digital I/O TA3 CCR2 capture: CCI2A input, compare: Out2
P8.3/A22/TA3CLK/L46						ADC analog input A22 LCD drive pin 46 for either segment or common output General-purpose digital I/O TA3 input clock

MSP432P4xx pin attributes descriptions

SIGNAL NAME	PIN (PZ)	Arduino	GPIO	ADC	Timer	UART	I2C	SPI	Clock	Port Mapper	Comparator	LCD
P8.4/A21/L45	48	43	P8.4	A21								L45
P8.5/A20/L44	49	41	P8.5	A20								L44
P8.6/A19/L19	50	57	P8.6	A19								L19
P8.7/A18/L18	51	58	P8.7	A18								L18
P9.0/A17/L17	52	42	P9.0	A17								L17
P9.1/A16/L16	53	59	P9.1	A16								L16
P9.2/TA3.3/L33	74	45	P9.2		TA3.3							L33
P9.3/TA3.4/L32	75	62	P9.3		TA3.4							L32
P9.4/UCA3STE/L43	96	49	P9.4					UCA3STE				L43
P9.5/UCA3CLK/L42	97	66	P9.5					UCA3CLK				L42
P9.6/UCA3RXD/UCA3SOMI/L41	98	50	P9.6			UCA3RXD		UCA3SOMI				L41
P9.7/UCA3TXD/UCA3SIMO/L40	99	67	P9.7			UCA3TXD		UCA3SIMO				L40
P10.0/UCB3STE/L39	100	54	P10.0					UCB3STE				L39
P10.1/UCB3CLK/L38	1	70	P10.1					UCB3CLK				L38
P10.2/UCB3SDA/UCB3SIMO/L37	2	55	P10.2				UCB3SDA	UCB3SIMO				L37

SIGNAL NAME	Debug	Power	RTC	Reference	System	DESCRIPTION
P8.4/A21/L45						ADC analog input A21 LCD drive pin 45 for either segment or common output General-purpose digital I/O
P8.5/A20/L44						ADC analog input A20 LCD drive pin 44 for either segment or common output General-purpose digital I/O
P8.6/A19/L19						ADC analog input A19 General-purpose digital I/O
P8.7/A18/L18						ADC analog input A18 General-purpose digital I/O
P9.0/A17/L17						ADC analog input A17 General-purpose digital I/O
P9.1/A16/L16						ADC analog input A16 General-purpose digital I/O
P9.2/TA3.3/L33						LCD drive pin 33 for either segment or common output General-purpose digital I/O TA3 CCR3 capture: CCI3A input, compare: Out3
P9.3/TA3.4/L32						LCD drive pin 32 for either segment or common output General-purpose digital I/O TA3 CCR4 capture: CCI4A input, compare: Out4
P9.4/UCA3STE/L43						LCD drive pin 43 for either segment or common output General-purpose digital I/O Slave transmit enable for eUSCI_A3 SPI mode
P9.5/UCA3CLK/L42						LCD drive pin 42 for either segment or common output General-purpose digital I/O Clock signal input for eUSCI_A3 SPI slave mode. Clock signal output for eUSCI_A3 SPI master mode
P9.6/UCA3RXD/UCA3SOMI/L41						LCD drive pin 41 for either segment or common output General-purpose digital I/O Slave out, master in for eUSCI_A3 SPI mode Receive data for eUSCI_A3 UART mode
P9.7/UCA3TXD/UCA3SIMO/L40						LCD drive pin 40 for either segment or common output General-purpose digital I/O Slave in, master out for eUSCI_A3 SPI mode Transmit data for eUSCI_A3 UART mode
P10.0/UCB3STE/L39						LCD drive pin 39 for either segment or common output General-purpose digital I/O
P10.1/UCB3CLK/L38						LCD drive pin 38 for either segment or common output General-purpose digital I/O Clock signal input for eUSCI_B3 SPI slave mode. Clock signal output for eUSCI_B3 SPI master mode
P10.2/UCB3SDA/UCB3SIMO/L37						LCD drive pin 37 for either segment or common output General-purpose digital I/O I2C data in eUSCI_B3 I2C mode Slave in, master out for eUSCI_B3 SPI mode

MSP432P4xx pin attributes descriptions

SIGNAL NAME	PIN (PZ)	Arduino	GPIO	ADC	Timer	UART	I2C	SPI	Clock	Port Mapper	Comparator	LCD
P10.3/UCB3SCL/UCB3SOMI/L36	3	71	P10.3				UCB3SCL	UCB3SOMI				L36
P10.4/TA3.0/C0.7/L35	24	56	P10.4		TA3.0						C0.7	L35
P10.5/TA3.1/C0.6/L34	25	72	P10.5		TA3.1						C0.6	L34
PJ.0/LFXIN	41		PJ.0						LFXIN			
PJ.1/LFXOUT	42		PJ.1						LFXOUT			
PJ.2/HFXOUT	85		PJ.2						HFXOUT			
PJ.3/HFXIN	86		PJ.3						HFXIN			
PJ.4/TDI	92		PJ.4									
PJ.5/SWO	93		PJ.5									
VCORE	12											
DVCC1	13											
VSW	14											
DVSS1	15											
AVSS3	40											
AVSS1	43											
DCOR	44								DCOR			
AVCC1	45											
DVSS2	72											
DVCC2	73											
DVSS3	82											
NMI	83											
AVSS2	84											
AVCC2	87											
SWDIOTMS	94											
SWCLKTCK	95											
3.3V		1										
5V		21										
GND		20										
GND		22										
RST		16										

MSP432P4xx pin attributes descriptions

SIGNAL NAME	Debug	Power	RTC	Reference	System	DESCRIPTION
P10.3/UCB3SCL/UCB3SOMI/L36						LCD drive pin 36 for either segment or common output General-purpose digital I/O I2C clock in eUSCI_B3 I2C mode Slave out, master in for eUSCI_B3 SPI mode
P10.4/TA3.0/C0.7/L35						Comparator_E0 input 7 LCD drive pin 35 for either segment or common output General-purpose digital I/O TA3 CCR0 capture: CCI0A input, compare: Out0
P10.5/TA3.1/C0.6/L34						Comparator_E0 input 6 LCD drive pin 34 for either segment or common output General-purpose digital I/O TA3 CCR1 capture: CCI1A input, compare: Out1
PJ.0/LFXIN						Input for low-frequency crystal oscillator LFXT General-purpose digital I/O
PJ.1/LFXOUT						Output of low-frequency crystal oscillator LFXT General-purpose digital I/O
PJ.2/HFXOUT						Output for high-frequency crystal oscillator HFXT General-purpose digital I/O
PJ.3/HFXIN						Input for high-frequency crystal oscillator HFXT General-purpose digital I/O
PJ.4/TDI	TDI					JTAG test data input General-purpose digital I/O
PJ.5/SWO	SWO					Serial wire trace output JTAG test data output General-purpose digital I/O
VCORE		VCORE				Regulated core power supply (internal use only, no external current loading)
DVCC1		DVCC1				Digital power supply
VSW		VSW				DC/DC converter switching output
DVSS1		DVSS1				Digital ground supply
AVSS3		AVSS3				Analog ground supply
AVSS1		AVSS1				Analog ground supply
DCOR						DCO external resistor pin
AVCC1		AVCC1				Analog power supply
DVSS2		DVSS2				Digital ground supply
DVCC2		DVCC2				Digital power supply
DVSS3		DVSS3				Must be connected to ground
NMI					NMI	External nonmaskable interrupt External reset (active low)
AVSS2		AVSS2				Analog ground supply
AVCC2		AVCC2				Analog power supply
SWDIOTMS	SWDIOTMS					Serial wire data input/output (SWDIO)/JTAG test mode select (TMS)
SWCLKTCK	SWCLKTCK					Serial wire clock input (SWCLK)/JTAG clock input (TCK)
3.3V						
5V						
GND						
GND						
RST						